

REMARKS

Summary of Office Action

Claims 1-37 are pending in the above-identified patent application.

The Examiner has rejected claims 1-3, 5-10, 16-19 and 21-26 under 35 U.S.C. 102(e) as allegedly being anticipated by Lee et al. U.S. Patent 6,266,799. Claim 11 has been rejected under 35 U.S.C. 103(a) as allegedly being obvious from Lee '799 in view of Li et al. U.S. Patent 6,693,985. Claims 12-15 have been rejected under 35 U.S.C. 103(a) as allegedly being obvious from Lee '799 and Li '985, further in view of Wang et al. U.S. Patent 6,292,116.

Each of claims 4, 20 and 27-37 has been objected to as depending from a rejected base claim, but allowable subject matter has been indicated.

Summary of Applicants' Reply

Applicants note with appreciation the indication of allowable subject matter in claims 4, 20 and 27-37, and hereby expressly reserve the right to rewrite any one or more of claims 4, 20 and 27-37 in independent form should its respective base claim ultimately not be allowed.

Applicants have amended claims 1, 16 and 25 in order to more particularly define the invention.

The Examiner's rejections are respectfully traversed.

Applicants' Reply

Claims 1-3, 5-10, 16-19 and 21-26 have been rejected under 35 U.S.C. 102(e) as allegedly being anticipated by Lee et al. U.S. Patent 6,266,799. Claim 11 has been rejected under 35 U.S.C. 103(a) as allegedly being obvious from Lee '799 in view of Li et al. U.S. Patent 6,693,985. Claims 12-15 have been rejected under 35 U.S.C. 103(a) as allegedly being obvious from Lee '799 and Li '985, further in view of Wang et

al. U.S. Patent 6,292,116. These rejections are respectfully traversed.

As previously noted, applicants' invention, as defined by independent claims 1 and 16, is directed to circuitry and a method for extracting data from a data signal having a data rate that is twice the frequency of a reference clock signal. A first phase-shifted version of the reference clock signal is derived that is synchronized with a rising edge (i.e., a 0-to-1 level transition) of the data signal. The data signal is sampled in a predetermined phase relationship to this first phase-shifted version to extract a first partial stream of data. A second phase-shifted version of the reference clock signal is also derived that is synchronized with a falling edge (i.e., a 1-to-0 level transition) of the data signal. The data signal is further sampled in a predetermined phase relationship to this second phase-shifted version to extract a second partial stream of data. Claims 1 and 16, as amended, define this second sampling as occurring "in a predetermined phase relationship to the second phase-shifted version of the reference clock signal, while the" first sampling is occurring "in a predetermined phase relationship to the first phase-shifted version of the reference clock signal."

Applicants' invention, as defined by independent claim 25, is directed to an apparatus for receiving an information signal. Claim 25, as amended, similarly recites that "one of the two retimed data output signals [is] produced using a first respective recovered clock signal while the other of the two retimed data output signals is being produced using a second respective recovered clock signal."

The amendments are fully supported in the specification. For example, Paragraph [0130] states that "[o]ne phase detector 160a can track the 0-to-1 level changes in the data signal, while the other phase detector 160b can

track the 1-to-0 level changes in the data signal" (emphasis added).

Applicants respectfully submit that Lee '799 does not show or suggest processing of a second signal with one phase shifted version of a reference clock that is synchronized with transitions of one polarity while a first signal is being processed with another phase shifted version of the reference clock that is synchronized with transitions of an opposite polarity. Rather in Lee, all phases of the reference clock are used to process all transitions, to determine if the clock is synchronized with the data.

This is done in Lee by sampling each transition with four phases of the clock, two of which are advanced (by two different phase angles) to lead the nominal transition time, and two of which are retarded (by the same two different phase angles) to lag the nominal transition time. If the clock is synchronized with the data, either all four samples will be the same (if the data before and after the transition time are the same, meaning no transition actually occurred) or the data sampled by the two advanced phases will have one value and the data sampled by the two retarded phases will have the opposite value (where a transition actually occurred). If some other result is obtained, such as three samples having one value and one sample having the opposite value, then the clock is misaligned relative to the data.

The two examples in Lee cited by the Examiner -- Case A of FIG. 7A and Case A of FIG. 8A) -- show this. Although in FIG. 7A the transition is a 0-1 transition and in FIG. 8A the transition is a 1-0 transition, in both drawings all four phases are nominally synchronized, in predetermined phase relationships, with the same transition. Thus, in Lee, at any one transition time, all phases are nominally synchronized with one transition, unlike applicants' claimed invention in which some phases are synchronized with transitions of one polarization "while" (i.e., at the same

time as) other phases are synchronized with transitions of the other polarization.

For at least the foregoing reasons, applicants respectfully submit that independent claims 1, 16 and 25 are patentable. Each of claims 2, 3, 5-15, 17-19, 21-24 and 26 depends, directly or indirectly, from one of independent claims 1, 16 and 25, and therefore each is patentable as well. Similarly, each of allowable but objected-to claims 4, 20 and 27-37 depends directly or indirectly from one of claims 1, 16 and 25, and is patentable in current form for that reason.

Conclusion

In view of the foregoing, applicants respectfully submit that this application, including claims 1-37, as amended, is in condition for allowance. Reconsideration and allowance of this application are respectfully requested.

Respectfully submitted,

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